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LIST OF FIGURES

I.   **INTRODUCTION**

The DAQ-16 is a high speed data acquisition adapter for IBM AT and compatible machines offering eight differential analog input channels with 16-bit resolution, two analog output channels with 12-bit resolution, and four digital input/output lines. Other features of the DAQ-16 include:

Analog to Digital Converter

*   100 KHz maximum sampling rate.

*   Bipolar input ranges of ±2.5, ±5, and ±10 volts.

*   Unipolar input ranges of 0 to +2.5, 0 to +5, and 0 to +10 volts.

*   Selectable gains of 1, 10, and 100.

*   Two DMA channels for continuous acquisition.

*   Internal or external clock and trigger.

Digital to Analog Converters

*   Two independent analog output channels

*   Output ranges of 0 to +5 and ±5 volts.

*   Internal or external voltage reference.

Other Features

*   Interrupt on one of four sources including an external interrupt input.

*   High density D-62 connector for reduced noise.

II.   **BOARD DESCRIPTION**

A layout of the DAQ-16 is shown in figure 1. The base address of the adapter is selected using switches SW1 and SW2. The operating mode of the DAQ-16 is controlled by jumpers J1 - J7 while DMA and interrupt selections are set with jumpers J8 - J11. Connection to external equipment is made through the high density 62-pin connector CN1.
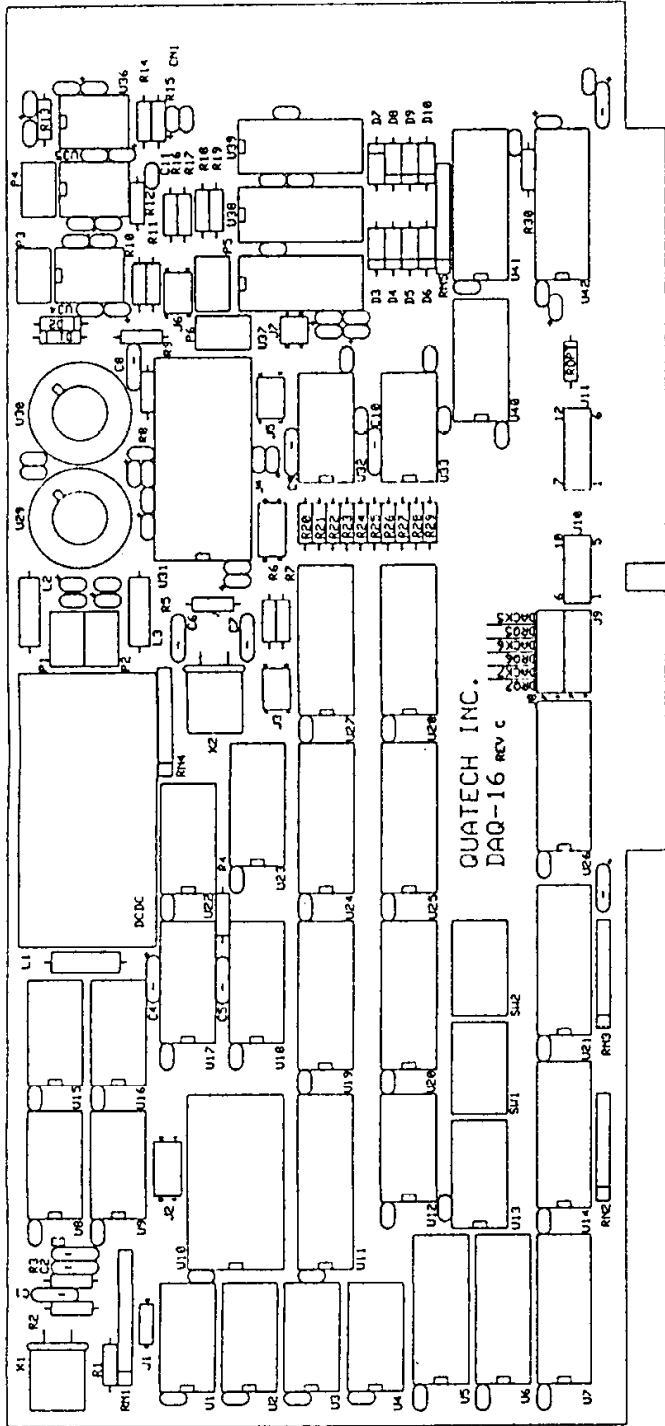
Figure 1.   DAQ-16 board layout.

III. **SYSTEM OVERVIEW**

Analog to digital converter

The analog to digital (A/D) section of the DAQ-16 accepts up to 8 differential inputs from the D-62 connector. These inputs pass through a dual 8-to-1 multiplexer circuit which selects the channel to be converted. The selected input is then amplified and presented to the A/D converter to be digitized. The digital output of the A/D is latched into a buffer to be read by the computer. This sequence is outlined in the diagram below.

```
 +-----------+      +-----+     +-----+     +-----+     +----+
 | CONNECTOR +---+ Mux +---+ Amp +---+ A/D +---+ PC |
 +-----------+      +-----+     +-----+     +-----+     +----+
```
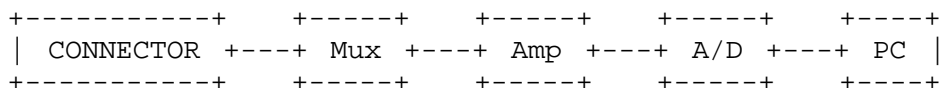
The multiplexer circuit selects one of the 8 differential channels to be input to the A/D converter. The channel is software selected through the DAQ-16's control word register. The typical characteristics of the multiplexer circuit are:

$$
\begin{array}{rl}
\text{input resistance:} & 1.5 \text{ K\_} \\
\text{switching time:} & 0.5 \text{ µs} \\
\text{settling time:} & 3.5 \text{ µs}
\end{array}
$$

The amplifier stage of the A/D converter circuit performs two functions: 1) amplify low level input signals and 2) convert this input signal into a voltage range acceptable to the A/D converter. The amplifier circuit is controlled by jumpers J6 and J7. Figure 4 below gives recommended jumper settings for various input voltage ranges. Where these settings are only suggestions, it is the user's responsibility to guarantee that the maximum input voltage multiplied by the gain setting selected by jumper J7 does not exceed the A/D voltage range set by jumper J6.

```
        J7                      J7                      J7
   +------+                +------+                +------+
  3|  _--_ |4             3| _ +_ |4             3| _+ _ |4
  1| _  _  |2             1| _ +_ |2             1| _+ _ |2
   +------+                +------+                +------+
    gain = 1               gain = 10              gain = 100
```

Figure 2.   A/D converter input gain selection.

```
        J6                      J6                      J6
   +---------+             +---------+             +---------+
  4| _  _--_ |6           4| _--_  _ |6           4| _--_  _ |6
  1| _  _--_ |3           1| _--_  _ |3           1| _  _--_ |3
   +---------+             +---------+             +---------+
   10 Volt range           5 Volt range           2.5 Volt range
```
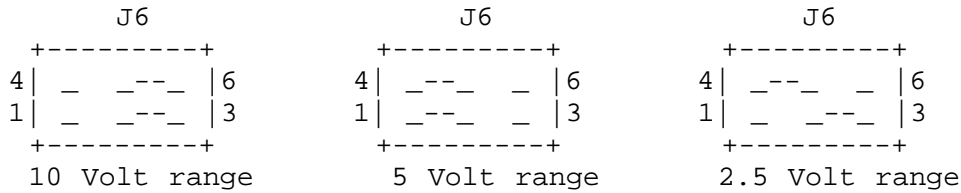
Figure 3.   A/D converter input range selection.

max. input voltage					
unipolar	bipolar	amp. gain	J7	A/D range	J6
+10.000	±10.000	1	3-4 *	10 V	2-3,5-6 *
+5.000	±5.000	1	3-4	5 V	1-2,4-5
+2.500	±2.500	1	3-4	2.5 V	2-3,4-5
+1.000	±1.000	10	2-4	10 V	2-3,5-6
+0.500	±0.500	10	2-4	5 V	1-2,4-5
+0.250	±0.250	10	2-4	2.5 V	2-3,4-5
+0.100	±0.100	100	1-3	10 V	2-3,5-6
+0.050	±0.050	100	1-3	5 V	1-2,4-5
+0.025	±0.025	100	1-3	2.5 V	2-3,4-5

*Indicates factory setting

Figure 4.   Recommended A/D converter configurations.

```
+==========================================================+
|   WARNING:                                               |
|       It is the user's responsibility to guarantee       |
|    that the maximum input voltage multiplied by the      |
|    gain setting selected by jumper J7 does not           |
|    exceed the A/D voltage range set by jumper J6.        |
+==========================================================+
```
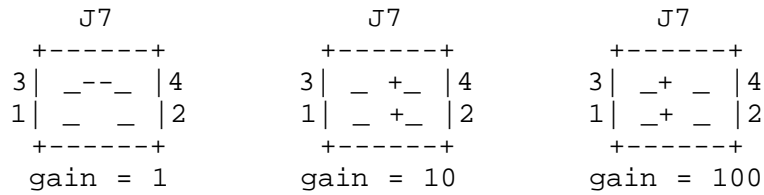
The final stage of the A/D converter circuit is the A/D converter IC. The converter must be configured for unipolar or bipolar input voltages and for binary or 2's complement data conversion. These options are selected using jumper J5 as shown in figure 5 below.

```
         J5                      J5
    +---------+             +---------+
  4| _  _  _ |6           4| _  _  _ |6
  1| _--_  _ |3           1| _  _--_ |3
    +---------+             +---------+
      Unipolar               Bipolar


         J5                      J5
    +---------+             +---------+
  4| _--_  _ |6           4| _  _--_ |6
  1| _  _  _ |3           1| _  _  _ |3
    +---------+             +---------+
       Binary             2's complement
```
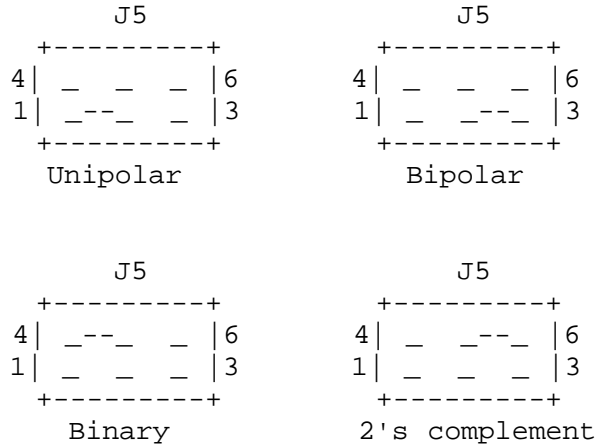
Figure 5.   A/D converter operating mode selections.

To simplify the following discussions, a new variable, Vmax, is introduced. Vmax is defined as the maximum input voltage amplitude and is equal to the A/D range selected by jumper J6 divided by the amplifier gain defined by jumper J7. In equation form

$$Vmax = \frac{A/D \ range}{amp. \ gain}$$

When configured for unipolar operation, the input voltage may range from 0 volts (analog ground) to Vmax volts as defined above. When configured for bipolar operation, the input voltage may range from -Vmax volts to +Vmax volts.

The digital "code" generated for any specific voltage is dependent upon the operating mode: unipolar or bipolar; and the data conversion format: binary or 2's complement. Binary conversion will result in unsigned integers ranging from 0 to 65,535 while 2's complement conversion will produce signed integers ranging from -32,768 to +32,767. A table of example values is given in the figure below. Unipolar entries marked n/a are not applicable because the voltage is outside of the unipolar voltage range.

```
+---------+-------------------+-------------------+
|         |       Binary      |   2's complement  |
| Voltage +---------+---------+---------+---------+
|         | unipolar | bipolar | unipolar | bipolar |
+---------+---------+---------+---------+---------+
|  -Vmax  |   n/a   |    0    |   n/a   | -32,768 |
|    .    |    .    |    .    |    .    |    .    |
|    .    |    .    |    .    |    .    |    .    |
| -Vmax/2 |   n/a   | +16,384 |   n/a   | -16,384 |
|    .    |    .    |    .    |    .    |    .    |
|    .    |    .    |    .    |    .    |    .    |
|    0    |    0    | +32,768 | -32,768 |    0    |
|    .    |    .    |    .    |    .    |    .    |
|    .    |    .    |    .    |    .    |    .    |
| +Vmax/2 | +32,768 | +49,152 |    0    | +16,384 |
|    .    |    .    |    .    |    .    |    .    |
|    .    |    .    |    .    |    .    |    .    |
|  +Vmax  | +65,535 | +65,535 | +32,767 | +32,767 |
+---------+---------+---------+---------+---------+
```

Figure 6.   A/D conversion format examples.

In order to calculate the actual input voltage from the digital "code" provided by the DAQ-16, the user must know the configuration used to acquire the data. Given this information, the input voltage can be calculated using the equations below:

Unipolar, binary

$$input = \left[\frac{CODE}{65,536} \right] * Vmax$$

Bipolar, binary

$$input = 2 * \left[\frac{CODE}{65,536} - \frac{1}{2} \right] * Vmax$$

Unipolar, 2's complement

$$input = \left[\frac{CODE}{65,536} + \frac{1}{2} \right] * Vmax$$

Bipolar, 2's complement

$$input = 2 * \left[\frac{CODE}{65,536} \right] * Vmax$$

Digital to analog converters

        The digital to analog (D/A) section of the DAQ-16
consists of two independent 12-bit multiplying D/A
converters, and two independent two-stage output
amplifiers. Digital data, output to the D/A converter by
the CPU, is converted to an analog voltage by the D/A
converter, amplified by the output amplifiers, and output
to the 62 pin connector CN1. This sequence is outlined
in the diagram below.

```
    +----+      +-----+      +-----+      +-----------+
    | PC +----+ DAC +----+ AMP +----+ CONNECTOR |
    +----+      +-----+      +-----+      +-----------+
```
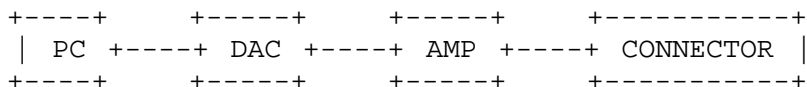
        The D/A converters used on the DAQ-16 are 12-bit
resolution converters. Of the 16 bits written to the
D/A, only the 12 least significant bits (D0 - D11) are
used for the conversion. The 4 most significant bits
(D12 - D15) are ignored.

        The DAQ-16 implements multiplying D/A converters
which makes the analog output proportional to a reference
voltage applied to the D/A. Under normal circumstances,
the reference voltage should be applied from the internal
+5V reference source. An external reference voltage may
also be supplied to the D/A. This input from the D-62
connector should not exceed 5 volts and has a typical
input impedance of 7.5K_. The D/A reference voltage
source is selected using jumper J3 as illustrated in
figure 7.

```
              D/A channel 0 reference
                        |
     internal source --+   |   +-- external source
                    +---------+
                 4| _  _  _ |6
         J3    1| _  _  _ |3
                    +---------+
     internal source --+   |   +-- external source
                        |
              D/A channel 1 reference
```
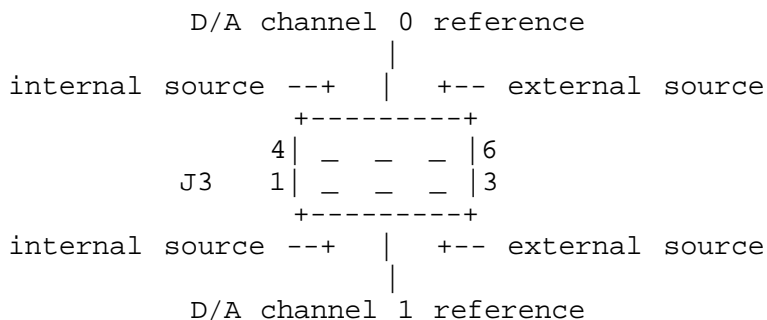
  Figure 7.   D/A converter reference voltage selection.

        The D/A converter channels may also be operated in
unipolar mode, 0 to +5 volts, or bipolar mode, -5 to +5
volts.   The output mode is selected using jumper J4 as
shown below.

        In addition, a gain selection jumper is provided to
select an output gain of 1 or 2.   When using an external
voltage reference, this gain can be used to amplify the
D/A output for small reference voltages.

WARNING
        **When the internal voltage reference is used,
the D/A gain MUST be set to the gain = 1 position.**


```
                          J4
                +------------+
              5|  _+ _+ _+ _+|8
              1|  _+ _+ _+ _+|4
                +------------+
     channel 0 select --+   |   |   +-- channel 1 gain
        channel 0 gain -----+   +----- channel 1 select


                +------------+-------------+
                |  channel 0  |  channel 1  |
        +----------+------------+-------------+
        |  bipolar  | connect 1-5 | connect 3-7 |
        | unipolar  |    open 1-5 |    open 3-7 |
        +----------+------------+-------------+
        | gain = 1 | connect 2-6 | connect 4-8 |
        | gain = 2 |    open 2-6 |    open 4-8 |
        +----------+------------+-------------+
```

        Figure 8.   D/A converter mode selections.

        When configured for unipolar operation, the output
voltage can be calculated from the equation:

$$A_{out} = V_{ref} * \frac{CODE}{4096} * gain$$

For bipolar operation, the equation becomes:

$$A_{out} = V_{ref} * \left[\frac{CODE}{2048} - 1 \right] * gain$$

Digital input/output

The DAQ-16 offers four bits of digital output and four bits of digital input for control/monitoring of external digital devices. The four digital output lines are LS TTL compatible and will initialize low (0 volts) on power-up. The four digital inpu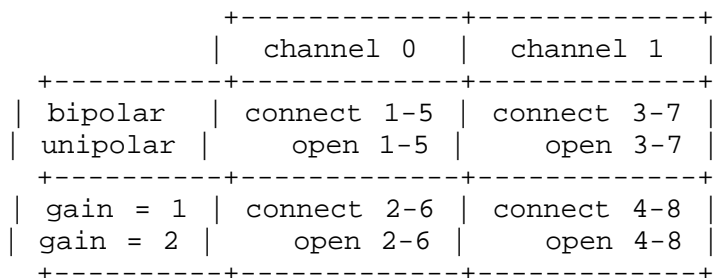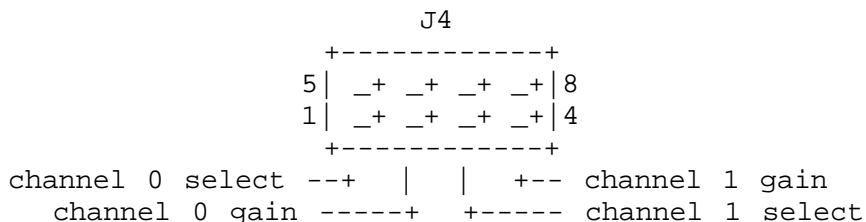ts are also LS TTL compatible. There is no termination provided on the digital input lines and a read of an unused digital input will result in an indeterminate value.

IV. **ADDRESSING**

The DAQ-16 uses 16 consecutive I/O address locations in the range 0 to 0FFFFH. Two six-position switches (SW1 and SW2) are used to select the base address. SW1 controls address lines A15 - A10, and SW2 controls A9 - A4. Address lines A3 - A0 are used internally by the DAQ-16 to select which register to access.

When selecting a base address for the DAQ-16, an address selection switch in the "OFF" position corresponds to an address bit of "1" while a switch in the "ON" position corresponds to an address bit of "0". The base address of the DAQ-16 must be set on a 16 byte boundary, meaning A3 - A0 are "0".

The address of the DAQ-16 as shipped from the factory is 0300H. This setting and other examples are shown in the figures below.

```
       +-------------------+           +-------------------+
    On|  +-++-++-++-++-++-+  |        On|  +-++-++-++-++-++-+  |
      |  |_||_||_||_||_||_|  |          |  |  || ||_||_||_||_|  |
      |  |  || || || || ||  |          |  |_||_|| || || ||  |  |
   Off|  +-++-++-++-++-++-+  |       Off|  +-++-++-++-++-++-+  |
      |  1  2  3  4  5  6   |          |  1  2  3  4  5  6   |
       +-------------------+           +-------------------+
              SW1                             SW2
```
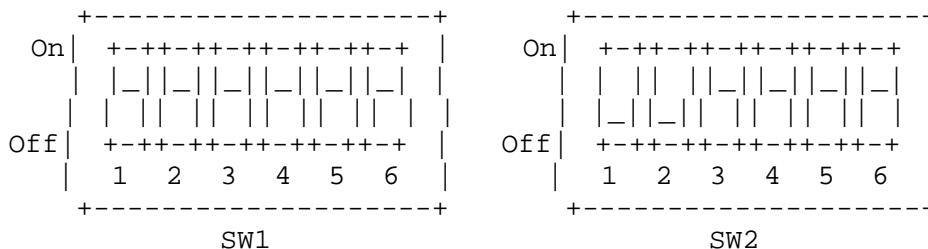
Figure 9. Base address selection switches.

```
          1   2   3   4     5   6   1   2     3   4   5   6
   On  +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
       |_||_||_||_|     |_||_|| || |     |_||_||_||_|
       |  ||  ||  ||  |     |  ||  ||_||_|     |  ||  ||  || |
   Off +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
        0   0   0   0     0   0   2   1     0   0   0   0
                  0                 3                 0    0 = 0300H


          1   2   3   4     5   6   1   2     3   4   5   6
   On  +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
       |_||_||_||_|     |_||_|| || |     |_||_|| || |
       |  ||  ||  || |     |  ||  ||_||_|     |  ||  ||_||_|
   Off +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
        0   0   0   0     0   0   2   1     0   0   2   1
                  0                 3                 3    0 = 0330H


          1   2   3   4     5   6   1   2     3   4   5   6
   On  +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
       |_||_||_|| |     |_|| || ||_|     |  || || ||_|
       |  ||  ||  ||_|     |  ||_||_|| |     |_||_||_|| |
   Off +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
        0   0   0   1     0   4   2   0     8   4   2   0
                  1                 6                 E    0 = 16E0H


          1   2   3   4     5   6   1   2     3   4   5   6
   On  +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
       |_||_|| ||_|     |  ||_|| ||_|     |_|| || ||_|
       |  || ||_|| |     |_|| ||_|| |     |  ||_||_|| |
   Off +-++-++-++-+     +-++-++-++-+     +-++-++-++-+
        0   0   2   0     8   0   2   0     0   4   2   0
                  2                 A                 6    0 = 2A60H
```

Figure 10. Address selection examples.

iii

V.   **CLOCK   SELECTIONS**

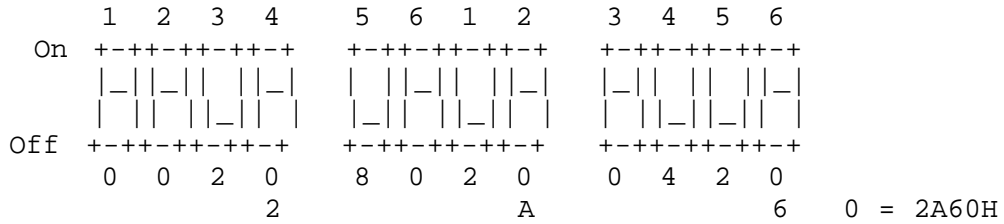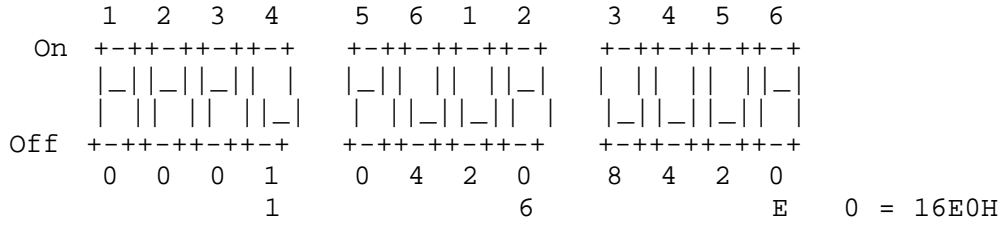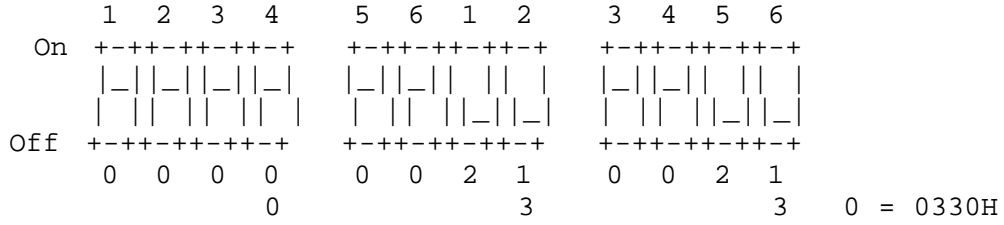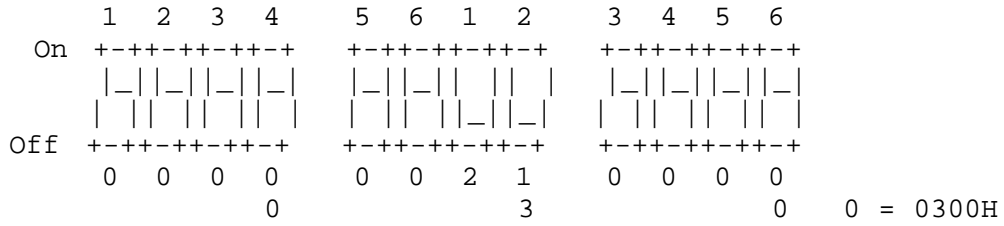The DAQ-16 is equipped with a programmable clock circuit to produce data sampling rates independent from the clock rate of the host computer. An onboard 8254 programmable interval timer, with a 10 MHz clock input and either two or three cascaded 16-bit timers, provides the sampling rate. This enables the sampling rate to be adjusted from 10 µs between samples to almost a year between samples, in as small as 100 ns increments.

The DAQ-16's sampling rate can also be generated from an external clock input. This external clock can be connected directly to the A/D converter or through a 16-bit pre-divider, the multi-function timer. Samples are taken on the low to high transition of the clock.

```
+========================================================+
|   WARNING:                                             |
|       For the DAQ-16, the maximum data sampling rate   |
|   is 10 µs.  This restricts clock frequency to a       |
|   maximum of 100 KHz.  Sampling rates in excess of     |
|   100 KHz may result in erratic operation and          |
|   unpredictable results.                               |
+========================================================+
```

The clock source, internal or external clock, is software selectable through the DAQ-16's control word register. The configuration of the clock source itself is controlled by jumper block J2 as shown in the figure below.

```
  +------------------------------------+----------+
  | Description                        |    J2    |
  +------------------------------------+----------+
  | Internal timer - 2 timers cascaded | 1-2,6-7     *  |
  |                - 3 timers cascaded | 2-6,7-8  |
  | External timer - w/o pre-divider   | 1-2,3-4  |
  |                - with pre-divider  | 2-3,4-8  |
  +------------------------------------+----------+
         *Indicates  factory  setting
```

Figure 11. Clock source selections.

CLOCK SELECTIONS

Internal clocks

        Sampling rates for the internal clock can be
calculated using the following equation:

$$t = 100ns * [N1*N2]$$
$$or \quad f = 10MHz / [N1*N2]$$

where N1 is the low 16-bits of the clock divider, and N2
is the high 16-bits of the clock divider.   The following
criteria must be met when selecting values for N1 and N2:

$$2 \_ N1 \_ 65,535$$
$$2 \_ N2 \_ 65,535$$

$$N1 * N2 \_ 100$$

        Using the equations above, the minimum and maximum
data sampling rates for the internal clock can be
calculated.

    Maximum sampling rate:

    N1 = 2, N2 = 50

        $t = 100 \times 10^{-9} * [(2)*(50)]$
          $= 100 \times 10^{-9} * 100$
          $= 10$ μs

        $f = 10 \times 10^{6} / [(2)*(50)]$
          $= 10 \times 10^{6} / 100$
          $= 100$ KHz

    Minimum sampling rate:

    N1 = 65535, N2 = 65535

        $t = 100 \times 10^{-9} * [(65535)*(65535)]$
          $= 100 \times 10^{-9} * [4.295 \times 10^{9}]$
          $= 429.5$ sec

        $f = 10 \times 10^{6} / [(65535)*(65535)]$
          $= 10 \times 10^{6} / [4.295 \times 10^{9}]$
          $= 2.328$ mHz

CLOCK SELECTIONS

If extremely slow data sampling rates are needed, the third 8254 timer, the multi-function timer, can be cascaded with the other two to produce a 48-bit clock divider. The sampling rates are then calculated as follows:

$$t = 100ns * [N1*N2*N3]$$
$$or \quad f = 10MHz / [N1*N2*N3]$$

where N1 is the low 16-bits of the clock divider, N2 is the intermediate 16-bits of the clock divider, and N3 is the high 16-bits of the divider. The following criteria must be met when selecting values for N1, N2, and N3:

$$2 \_ N1 \_ 65,535$$
$$2 \_ N2 \_ 65,535$$
$$2 \_ N3 \_ 65,535$$

$$N1 * N2 * N3 \_ 100$$

When configured for a 48-bit divider, the first sampling period will be slightly longer than the others because the first clock period is required to load the initial value of the multi-function timer. The following equation calculates the additional time of the first period:

$$t_{add} = 100ns * [N1 * N2]$$

To minimize the amount of additional time required for the first sample, select clock dividers such that N1 and N2 are as small as possible and N3 is as large as possible.

CLOCK SELECTIONS

        Using the equations above, the minimum and maximum
data sampling rates and the amount of additional time
required for the first sample can be calculated.

    Maximum sampling rate:

      N1 = 2, N2 = 2, N3 = 25

        $t = 100 \times 10^{-9} * [(2)*(2)*(25)]$
          $= 100 \times 10^{-9} * 100$
          = 10 μs

        $f = 10 \times 10^{6} / [(2)*(2)*(25)]$
          $= 10 \times 10^{6} / 100$
          = 100 KHz

    $t_{add} = 100 \times 10^{-9} * [2 * 2]$
          $= 100 \times 10^{-9} * 4$
          = 400 ns

    Minimum sampling rate:

      N1 = 65535, N2 = 65535, N3 = 65535

        $t = 100 \times 10^{-9} * [(65535)*(65535)*(65535)]$
          $= 100 \times 10^{-9} * [2.815 \times 10^{14}]$
          $= 28.146 \times 10^{6}$ sec
           = 325 days, 18 hours, 23 minutes, 29 sec

        $f = 10 \times 10^{6} / [(65535)*(65535)*(65535)]$
          $= 10 \times 10^{6} / [2.815 \times 10^{14}]$
          = 35.529 nHz

    $t_{add} = 100 \times 10^{-9} * [65535 * 65535]$
          $= 100 \times 10^{-9} * [4.295 \times 10^{9}]$
          = 429.5 sec

External clocks

The external clock input to the DAQ-16 is a TTL level (0 - 5 volt) signal. This input may be used to control the sampling rate directly, or it may be fed through a pre-divider, the multi-function timer, with the timer output controlling the A/D sampling rate.

When used to control the sampling rate directly, the frequency of the external clock input may be varied from DC to 100 KHz as long as the width of the low and high portions of the clock are a minimum of 1 µs each. The A/D conversion cycle will begin on each rising edge of the external clock input.

```
        +-- 1 µs min --+-- 1 µs min --+
        +--------------+              +---------
        |              |              |
   -----+              +--------------+
        +--------- 10 µs min ---------+
```
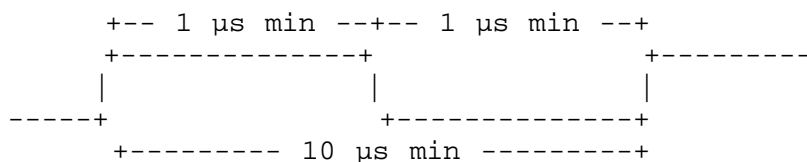
When the multi-function timer is used as a pre-divider, the frequency of the external clock input may be varied from DC to 10 MHz as long as the high portion of the clock is at least 30ns and the low portion is at least 50ns.

```
        +-- 30ns min --+-- 50ns min --+
        +--------------+              +---------
        |              |              |
   -----+              +--------------+
        +--------- 100ns min ---------+
```
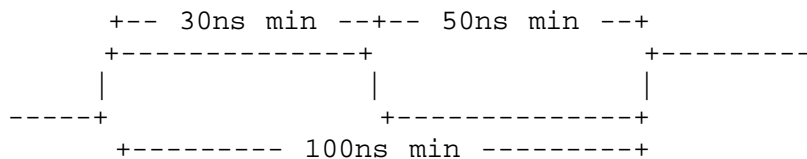
Except for the first period, the sampling rate of the DAQ-16 will be the external clock frequency divided by the count value written to the multi-function timer. Since one clock pulse is required to load the initial count value into the timer, the first sampling interval will be one clock cycle longer than the rest. The valid range of count values for the multi-function timer is 2 _ count _ 65,535 but the resulting sampling rate must be less than 100 KHz to assure proper operation of the A/D converter circuitry.

VI.   TRIGGER SELECTIONS

The DAQ-16 is capable of accepting an internal software trigger or an external hardware trigger. The trigger selection and trigger level bits in the DAQ-16 control word register select the trigger source and level. Upon reset, the trigger selection and trigger level bits default to the internal software trigger. When the internal trigger is used, an output to the start-of-conversion register will trigger the DAQ-16 to begin sampling the input.

For triggering off an external event, the DAQ-16 accepts a level sensitive, TTL compatible trigger input from the D-62 connector. The trigger level bit in the DAQ-16 control word register determines which TTL level is used to trigger the A/D converter to begin sampling.
When an internal clock source is used, a delay of not more than 225 ns will occur between the trigger and the first data sample. When an external clock is used, the delay will be dependent on the frequency and duty cycle of the clock input. If these delays are unacceptable, the clock and trigger circuitry can be bypassed and a start of conversion pulse can be input directly into the A/D circuitry with a maximum delay of 25 ns. If the user controls the start of conversion pulse directly, the sample will be taken on the low to high transition of the pulse, the pulse must have a duration of at least 10 µs, and the duty cycle must be between 5 and 80 percent.

```
                         J1
                    +---------+
                  1 | _  _  _ |3
                    +---------+


         +---------------------+------+
         | start-of-conversion |  J1  |
         +---------------------+------+
         | DAQ-16 controlled   | 1-2   *  |
         | user controlled     | 2-3  |
         +---------------------+------+
            *Indicates  factory  setting
```
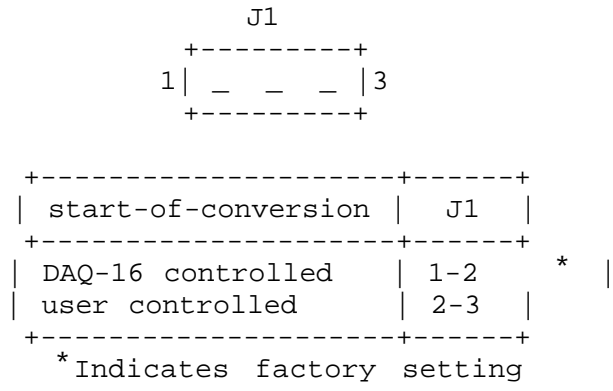
Figure 12.   Start of conversion selection.

VII.   **DIRECT MEMORY ACCESS**

        Direct Memory Access (DMA) transfers provide a way
of transferring data from the DAQ-16's A/D converter into
the personal computer's memory without using the Central
Processing Unit (CPU). DMA capability enables other
system software to be executed while data is being input
from the DAQ-16.

        The DAQ-16 actually implements two DMA channels.
The advantage of having two DMA channels is that one
channel can be transferring data while the second channel
is being programmed. When the first channel is finished,
the second channel will automatically take over and
continue the data transfer. The first channel can then
be re-programmed while the second channel is transferring
data. In this way, the DAQ-16 can acquire data
continuously until terminated by the user.

        The DAQ-16 supports 16-bit DMA transfers on channels
5, 6, and 7. The DMA channel(s) are selected by jumpers
J8 and J9 as shown in figure 13 below.

```
            DMA channel 1                      DMA channel 2
        +-----------------+               +-----------------+
        | _ _ _ _ _ _ |               | _ _ _ _ _ _ |
   J8   | _ _ _ _ _ _ |          J9   | _ _ _ _ _ _ |
        +-----------------+               +-----------------+
  DRQ7  --+  |  |  |  |  |        DRQ7  --+  |  |  |  |  |
 DACK7  -----+  |  |  |  |       DACK7  -----+  |  |  |  |
  DRQ6  --------+  |  |  |        DRQ6  --------+  |  |  |
 DACK6  -----------+  |  |       DACK6  -----------+  |  |
  DRQ5  -------------+  |        DRQ5  -------------+  |
 DACK5  ----------------+       DACK5  ----------------+
```
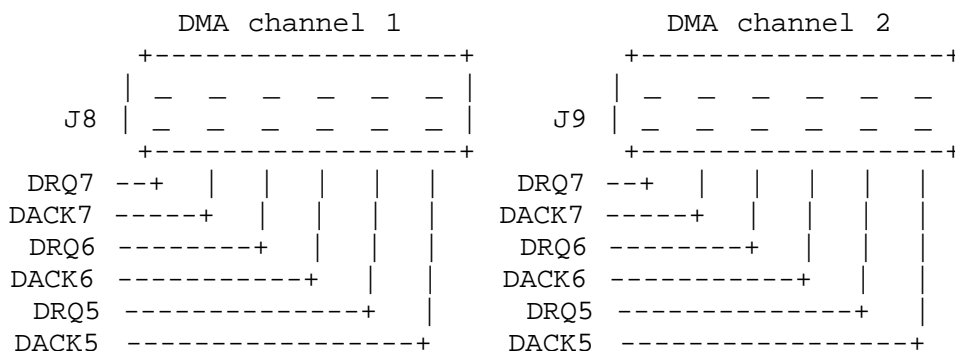
        Figure 13. DMA channel selections.

```
+=========================================================+
|   WARNING:                                              |
|        To properly implement the DMA capability, the    |
|   DRQ and DACK of a DMA channel must be jumpered to      |
|   the same number, i.e. DRQ 5 and DACK 5.  If both       |
|   DMA channels are to used, each channel must be         |
|   jumpered to a different number, i.e. DMA channel       |
|   1 is jumpered to DRQ 5 and DACK 5 and DMA channel      |
|   2 is jumpered to DRQ 7 and DACK 7.                     |
+=========================================================+
```

VIII.   **INTERRUPTS**

        The DAQ-16 is capable of generating an interrupt
from one of four sources: end of conversion signal, DMA
terminal count, multi-function timer output, or from the
external interrupt input. The interrupt source is
software selected through the DAQ-16 control word
register. The interrupt level is selected using the
jumpers J10 and J11 as shown in figure 14 below.

```
Interrupt
 source           J10                        J11
   |        +--------------+          +-----------------+
   +------|-_--_--_--_-|--------|-_--_--_--_--_--_  |
          | _  _  _  _  _ |          | _  _  _  _  _  _ |
          +--------------+          +-----------------+
   IRQ 10 --+  |  |  |  |    IRQ 2 --+  |  |  |  |  |
   IRQ 11 -----+  |  |  |    IRQ 3 -----+  |  |  |  |
   IRQ 12 --------+  |  |    IRQ 4 --------+  |  |  |
   IRQ 15 -----------+  |    IRQ 5 -----------+  |  |
   IRQ 14 -------------+    IRQ 6 -------------+  |
                             IRQ 7 -----------------+
```
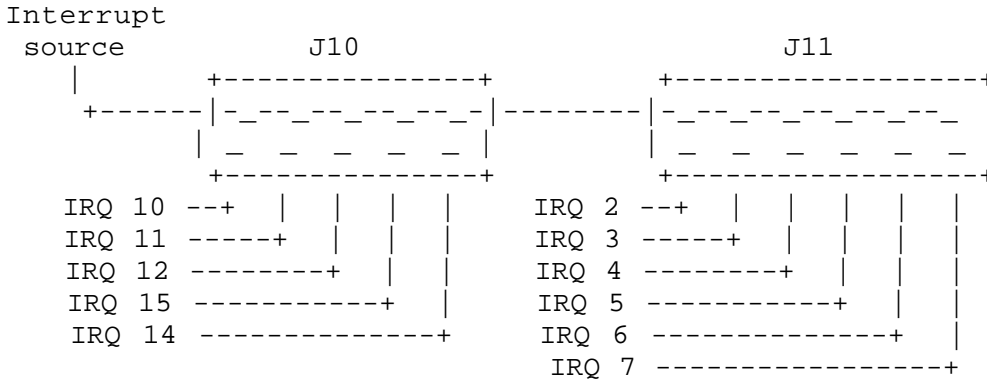
        Figure 14.   Interrupt level selections.

<u>External</u> <u>Interrupt</u>

        The external interrupt is a TTL compatible input
from the D-62 connector. An interrupt request is
generated on a high to low transition of this input.

IX.   CONFIGURATION   SUMMARY

A/D start conversion pulse - J1

```
+-------------------+------+
| Description       |  J1  |
+-------------------+------+
| DAQ-16 controlled | 1-2  *  |
| user controlled   | 2-3  |
+-------------------+------+
```

A/D sampling rate - J2

```
+----------------------------------+----------+
| Description                      |   J2     |
+----------------------------------+----------+
| Internal timer - 2 cascaded      | 1-2,6-7    *  |
|                 - 3 cascaded     | 2-6,7-8  |
| External timer - w/o pre-divider | 1-2,3-7  |
|                 - with pre-divider | 1-5,3-7  |
+----------------------------------+----------+
```

A/D conversion mode/data format - J5

```
+----------------+------+
| Description    |  J5  |
+----------------+------+
| Unipolar       | 1-2  *  |
| Bipolar        | 2-3  |
+----------------+------+
| Binary         | 4-5  *  |
| 2's complement | 5-6  |
+----------------+------+
```

Maximum input amplitude - J6

```
+-------------+----------+
| Description |   J6     |
+-------------+----------+
|  10 volts   | 2-3,5-6   *  |
|   5 volts   | 1-2,4-5  |
|  2.5 volts  | 2-3,4-5  |
+-------------+----------+
```

Input gain - J7

```
+-------------+------+
| Description |  J7  |
+-------------+------+
|    1        | 3-4  *  |
|   10        | 2-4  |
|  100        | 1-3  |
+-------------+------+
```

*Indicates factory settings.

D/A converter reference voltage - J3

```
+--------------------------+------+
| Description              |  J3  |
+--------------------------+------+
| DAC0 - internal reference | 1-2    *  |
|      - external reference | 2-3   |
| DAC1 - internal reference | 4-5    *  |
|      - external reference | 5-6   |
+--------------------------+------+
```

D/A converter output mode - J4

```
+----------------------+--------------+
| Description          |      J4      |
+----------------------+--------------+
| DAC0 - bipolar mode  | connect 1-5    *  |
|      - unipolar mode |    open 1-5   |
|      - gain = 1      | connect 2-6    *  |
|      - gain = 2      |    open 2-6   |
| DAC1 - bipolar mode  | connect 3-7    *  |
|      - unipolar mode |    open 3-7   |
|      - gain = 1      | connect 4-8    *  |
|      - gain = 2      |    open 4-8   |
+----------------------+--------------+
```

Interrupt level selection - J10,J11

```
+-------------+------+------+
| Description | J10  | J11  |
+-------------+------+------+
| IRQ 9 (2)   | 1-7  |      |
| IRQ 3       | 2-8  |      |
| IRQ 4       | 3-9  |      |
| IRQ 5       | 4-10 |      |
| IRQ 6       | 5-11 |      |
| IRQ 7       | 6-12 |      |
| IRQ 10      |      | 1-6  |
| IRQ 11      |      | 2-7  |
| IRQ 12      |      | 3-8  |
| IRQ 14      |      | 4-9  |
| IRQ 15      |      | 5-10 |
+-------------+------+------+
```

DMA channel selection - J8,J9

```
+--------------------------+-----------+-----------+
| Description              |    J8     |    J9     |
+--------------------------+-----------+-----------+
| DMA channel 0 - level 7  | 1-7,2-8   |           |
|                - level 6 | 3-9,4-10  |           |
|                - level 5 | 5-11,6-12 |           |
| DMA channel 1 - level 7  |           | 1-7,2-8   |
|                - level 6 |           | 3-9,4-10  |
|                - level 5 |           | 5-11,6-12 |
+--------------------------+-----------+-----------+
```

*Indicates factory settings.

X.   **Register   Description**

The DAQ-16 uses 16 consecutive I/O address locations in the range 0 to FFFFH.   The card utilizes these addresses for the registers shown in figure 15 below.

```
+--------+--------------------------------+
| Offset | Function / Access              |
+--------+--------------------------------+
|  0,1   | Control word register          |
|        |     16-bit read/write          |
|  2,3   |  Start conversion register     |
|        |     16-bit write only          |
|        | A/D data register              |
|        |     16-bit read only           |
|  4,5   | D/A channel 0 register          |
|        |     16-bit write only          |
|  6,7   | D/A channel 1 register          |
|        |     16-bit write only          |
|   8    |  Digital input/output register |
|        |     8-bit read/write           |
|   9    | Reserved                       |
|   A    | Reserved                       |
|   B    | Reserved                       |
|   C  * | Clock rate register (low)       |
|        |     8-bit read/write           |
|   D  * | Clock rate register (high)      |
|        |     8-bit read/write           |
|   E  * | Multi-function timer register   |
|        |     8-bit read/write           |
|   F  * | 8254 control word/status register |
|        |     8-bit read/write           |
+--------+--------------------------------+
```
   *These registers are contained in an 8254 counter

Figure 15.   DAQ-16 address map.

The base address of the DAQ-16 is defined by a pair of six-position switches SW1 and SW2.   For details on setting the base address, consult section IV.

REGISTER DESCRIPTION

Control word register

        The control word register defines and controls many
of the DAQ-16's data conversion functions.   This
register is 16-bit read/write.

```
         Write           Read                    Write           Read
        +-------+      +-------+               +-------+      +-------+
 D15 |  INT2  |      |  INT2  |          D7 |  RUN  |      |  RUN  |
        +-------+      +-------+               +-------+      +-------+
 D14 |  INT1  |      |  INT1  |          D6 |   0   |      |  EOC  |
        +-------+      +-------+               +-------+      +-------+
 D13 |  INT0  |      |  INT0  |          D5 |   0   |      | VALID |
        +-------+      +-------+               +-------+      +-------+
 D12 | DMAEN |      | DMAEN |          D4 |   0   |      |   0   |
        +-------+      +-------+               +-------+      +-------+
 D11 | DMACT |      | DMACH |          D3 |   0   |      |   0   |
        +-------+      +-------+               +-------+      +-------+
 D10 | LEVEL |      | LEVEL |          D2 | CHSL2 |      | CHSL2 |
        +-------+      +-------+               +-------+      +-------+
  D9 |  TRIG  |      |  TRIG  |          D1 | CHSL1 |      | CHSL1 |
        +-------+      +-------+               +-------+      +-------+
  D8 |  CLK   |      |  CLK   |          D0 | CHSL0 |      | CHSL0 |
        +-------+      +-------+               +-------+      +-------+
```


INT2,INT1,INT0 - controls the DAQ-16 interrupt source.

```
+------+------+------+-------------------------------+
| INT2 | INT1 | INT0 | DESCRIPTION                   |
+------+------+------+-------------------------------+
|   0  |   0  |   0  | Interrupt disabled            |
|   1  |   0  |   0  | Interrupt timer 2             |
|   1  |   0  |   1  | Interrupt on terminal count   |
|   1  |   1  |   0  | External interrupt            |
|   1  |   1  |   1  | Interrupt on end of conversion |
+------+------+------+-------------------------------+
```

DMAEN -enables / disables DMA. When set, logic 1, DMA
         transfers are enabled. See DMACT and DMACH.

DMACT -enables the multi-channel DMA capability of the
         DAQ-16. When set, logic 1, a terminal count on
         the active DMA channel causes DMA transfers to
         begin on the "stand-by" channel. When cleared,
         logic 0, DMA transfers halt when the terminal
         count is reached on the active channel. See
         DMACH and DMAEN.

DMACH -indicates which of the DAQ-16's DMA channels is
         currently active to transfer data. Logic 0
         indicates DMA channel 0, logic 1 indicates DMA
         channel 1. See DMAEN and DMACT.

REGISTER   DESCRIPTION

LEVEL -selects the edge of the external trigger input.
       When set, logic 1, A/D conversions will begin on
       the falling edge of the external trigger input.
       When cleared, logic 0, conversions will begin on
       the rising edge of the external trigger.
       IMPORTANT: LEVEL must be logic 0 when internal
       triggering is used.   See also TRIG.

TRIG   -selects between internal and external triggers.
       When set, logic 1, the external trigger is
       selected.   See also LEVEL.

CLK   -selects between internal and external clock
       sources.   When set, logic 1, the external clock
       source is selected.

RUN   - when set, logic 1, the A/D converter is placed in
       the 'run' mode and will begin converting data
       when a trigger is received.   RUN may be cleared
       at any time by writing a "0" to it.   When using
       DMA transfers, RUN is automatically cleared when
       a terminal count is received with DMACT set to
       "0".

EOC   -when set, indicates an end of conversion has
       taken place and the data is available in the A/D
       converter data register.

VALID -when set, logic 1, indicates at least one data
       sample was lost because it was read by the
       personal computer before the next sample was
       converted.   The data was lost because the
       sampling rate was to fast for the computer to
       acquire the data.   VALID is reset by writing to
       the start conversion register.

CHSL2, CHSL1, CHSL0 - select the multiplexer channel
       for the analog input signal.

```
+-------+-------+-------+-------------+
| CHSL2 | CHSL1 | CHSL0 | mux. channel |
+-------+-------+-------+-------------+
|   0   |   0   |   0   | channel 0   |
|   0   |   0   |   1   | channel 1   |
|   0   |   1   |   0   | channel 2   |
|   0   |   1   |   1   | channel 3   |
|   1   |   0   |   0   | channel 4   |
|   1   |   0   |   1   | channel 5   |
|   1   |   1   |   0   | channel 6   |
|   1   |   1   |   1   | channel 7   |
+-------+-------+-------+-------------+
```

REGISTER   DESCRIPTION

Start of conversion register

The start of conversion register performs two
functions:

1) When configured for internal triggering, writing a
"0" to this register generates the software
trigger, starting the data conversion process.

2) Writing a "0" to this register at any time resets
the VALID bit in the control word register.   This
allows the VALID bit to be reset at any time
during the conversion process or before the event
of an external trigger.

The start of conversion register is 16-bit write only.

DAC0 register

An output to this register causes the lower twelve
bits of data to be converted to an analog output on D/A
converter channel 0.   The four most significant bits of
data are ignored.   This register is 16-bit write only.
For more details on the D/A converter operation, see
section III.

DAC1 register

An output to this register causes the lower twelve
bits of data to be converted to an analog output on D/A
converter channel 1.   The four most significant bits of
data are ignored.   This register is 16-bit write only.
For more details on the D/A converter operation, see
section III.

REGISTER DESCRIPTION

The remaining four registers are contained in an 8254 counter/timer. The suggested operating modes and associated control words are discussed in the following section.

Clock rate register (low word)

The low word of the clock divider is contained in counter 0 of an 8254 counter/timer. The output of this counter is cascaded into the input of counter 1 to produce a 32-bit timer. Mode 2 must be selected for counter 0 with a minimum count of 2. See section V for details on clock selections and frequencies. This register is 8-bit read/write.

Clock rate register (high word)

The high word of the clock divider is contained in counter 1 of the 8254 counter/timer. Mode 2 must be selected for counter 1 with a minimum count of 2. See section V for details on clock selections and frequencies. This register is 8-bit read/write.

Multi-function timer register

The multi-function timer is implemented using counter 2 of the 8254 counter/timer. Mode 2 must be selected for this timer with a minimum count of 2. See section V for details on clock selections and frequencies. This register is 8-bit read/write.

8254 control word/status register

This register is used to program the mode and report the status of the 8254 counter/timer. This register is 8-bit read/write.

XI.   PROGRAMMING   THE 8254 COUNTER/TIMER

This section provides programming information for the 8254 counter / timer as implemented on the DAQ-16. For more details on the 8254, consult the Intel Microprocessor and Peripheral Handbook.

To program any of the counters contained in the 8254 counter / timer, three steps are required:

1. Write the configuration byte to the 8254 mode select / status register. This byte sets the operating mode of the selected counter.
2. Write the least significant byte of the count value to the selected counter register.
3. Write the most significant byte of the count value to the selected counter register.

The following examples illustrate the programming sequence for each of the counters in the 8254. The variable 'base_address' is the base address of the DAQ-16 as defined by the address selection switches.

Counter 0 - Clock rate register (low word)

```
        operating mode:  2
  minimum count value:  2
    configuration byte:
          +---+---+---+---+---+---+---+---+
          | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | = 34H
          +---+---+---+---+---+---+---+---+
```

Example:
    Program the value 2675H into the low word of the clock rate register.

```
        output    34H    to    base_address + 0FH
        output    75H    to    base_address + 0CH
        output    26H    to    base_address + 0CH
```

Example:
    Program the value 0008H into the low word of the clock rate register.

```
        output    34H    to    base_address + 0FH
        output    08H    to    base_address + 0CH
        output    00H    to    base_address + 0CH
```

PROGRAMMING   THE   8254

COUNTER/TIMER

Counter 1 - Clock rate register (high word)

```
        operating mode:   2
   minimum count value:   2
     configuration byte:
            +---+---+---+---+---+---+---+---+
            | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |  = 74H
            +---+---+---+---+---+---+---+---+
```

Example:
    Program the value 13A4H into the high word of the
clock rate register.

```
        output    74H    to    base_address + 0FH
        output    A4H    to    base_address + 0DH
        output    13H    to    base_address + 0DH
```

Example:
    Program the value FFFFH into the high word of the
clock rate register.

```
        output    74H    to    base_address + 0FH
        output    FFH    to    base_address + 0DH
        output    FFH    to    base_address + 0DH
```

Counter 2 - Multi-function timer register

```
        operating mode:   2
   minimum count value:   2
     configuration byte:
            +---+---+---+---+---+---+---+---+
            | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |  = B4H
            +---+---+---+---+---+---+---+---+
```

Example:
    Program the value 000AH into the multi-function timer
register.

```
        output    B4H    to    base_address + 0FH
        output    0AH    to    base_address + 0EH
        output    00H    to    base_address + 0EH
```

Example:
    Program the value 0100H into the multi-function timer
register.

```
        output    B4H    to    base_address + 0FH
        output    00H    to    base_address + 0EH
        output    01H    to    base_address + 0EH
```

XII.   **EXTERNAL   CONNECTIONS**

The DAQ-16 is equipped with a high density 62-pin
connector as shown below.

```
|                                    2 - CH1+
|                                    4 - CH2-
|        22          |               6 - CH4+
|  1           43 |                  8 - CH5-
|        23          |              10 - CH7+
|  2           44 |                 12 - AOUT0
|        24          |              14 - DOUT0
|  3           45 |                 16 - DOUT3
|        25          |              18 - EXT TRIG
|  4           46 |                 20 - DIN1
|        26          |              22 - CH0+
|  5           47 |                 24 - CH1-
|        27          |              26 - CH3+
|  6           48 |                 28 - CH4-
|        28          |              30 - CH6+
|  7           49 |                 32 - CH7-
|        29          |              34 - AOUT1
|  8           50 |                 36 - DOUT1
|        30          |              38 - EXT INT
|  9           51 |                 40 - DIN3
|        31          |              42 - DIN0
| 10           52 |                 43 - CH0-
|        32          |              45 - CH2+
| 11           53 |                 47 - CH3-
|        33          |              49 - CH5+
| 12           54 |                 51 - CH6-
|        34          |              53 - VREF0
| 13           55 |                 55 - VREF1
|        35          |              57 - DOUT2
| 14           56 |                 59 - EXT CLK
|        36          |              61 - DIN2
| 15           57 |
|        37          |
| 16           58 |
|        38          |               Analog  Ground
| 17           59 |              1, 3, 5, 7, 9, 11, 13,
|        39          |             44, 46, 48, 50, 52, 54
| 18           60 |
|        40          |
| 19           61 |               Digital  Ground
|        41          |              15, 17, 19, 21, 37, 39,
| 20           62 |               41, 56, 58, 60, 62
|        42          |
| 21
|
|
```

CH0-,CH0+,...,CH7-,CH7+ - are the analog inputs to the
     analog to digital converter.   Their amplitude and
     polarity depend upon jumper settings.   The input
     resistance of these lines is 1.5 K_ typical.   See
     section III for details.

AOUT0, AOUT1 - are the analog outputs from the digital to
     analog converters.   Their polarity and maximum
     amplitude depend on the jumper settings and voltage
     references.   The output resistance of the analog
     outputs is typically 70 _.   See section III for
     details.

VREF0, VREF1 - are the external voltage references for
     the digital to analog converters.   The input range
     is 0 to 5.5 volts with a no-load input resistance of
     7.5 K_.

EXT CLK, EXT TRG, EXT INT - are the external clock,
     trigger, and interrupt inputs respectively.   These
     inputs are TTL compatible.

DOUT0, DOUT1, DOUT2, DOUT3 - are the TTL compatible
     digital output lines.

DIN0, DIN1, DIN2, DIN3 - are the TTL compatible input
     lines.

XIII.   INSTALLATION

1. Select options by adjusting switch positions and jumper settings as described in the previous sections of this manual.

2. Turn system off.

3. Remove cover according to the instructions provided by the system manufacturer.

4. Install the DAQ-16 into any vacant slot. The board must be secured to the machine by installing the Option Retaining Bracket (ORB) screw.

5. Replace system cover according to the instructions provided by the system manufacturer.

XIV.   SPECIFICATIONS

Bus interface: ISA 16-bit bus

I/O address range: 0000H - FFFFH

Interrupt levels: IRQ 2,3,4,5,6,7,10,11,12,14,15

DMA levels: DRQ 5,6,7
                       DACK 5,6,7

Power requirements:

Power supply	I_t	I_{ms}
-5 volts	--	--
+5 volts	1069.0 mA	1204.9 mA
-12 volts	--	--
+12 volts	374.9 mA	491.4 mA

I_t Typical current
I_{ms} Maximum statistical current